## Search Results -

Terms	Documents
L1 same multiple same (empt\$3 or free)	5

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# Search History

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<u>L2</u> L1 same multiple same (empt\$3 or free)

5 <u>L2</u>

<u>L1</u> synchronous\$3 same asynchronous\$3 same (rate or speed)

1790 L1

# Search Results -

Terms	Documents	
L4 and bridge	0	

Database:

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L6

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# **Search History**

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Set Name Query side by side	Hit Count	Set Name result set
DB=EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR		
<u>L6</u> L4 and bridge	0	<u>L6</u>
DB=PGPB, USPT, USOC; PLUR=YES; OP=OR		
<u>L5</u> L4 and bridge	31	<u>L5</u>
<u>L4</u> L1 same multiple	231	<u>L4</u>
<u>L3</u> L1 same multiple same (empt\$3 or free)	5	<u>L3</u>
DB=PGPB; PLUR=YES; OP=OR		
<u>L2</u> L1 same multiple same (empt\$3 or free)	. 5	<u>L2</u>
<u>L1</u> synchronous\$3 same asynchronous\$3 same (rate or speed)	1790	<u>L1</u>

# Search Results -

Terms	Documents
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L6 L4 and bridge

DB=PGPB, USPT, USOC; PLUR=YES; OP=OR

L5 L4 and bridge

L4 L1 same multiple

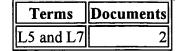
L3 L1 same multiple same (empt\$3 or free)

DB=PGPB; PLUR=YES; OP=OR

<u>L2</u> L1 same multiple same (empt\$3 or free)

L1 synchronous\$3 same asynchronous\$3 same (rate or speed)

## Search Results -



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Search:

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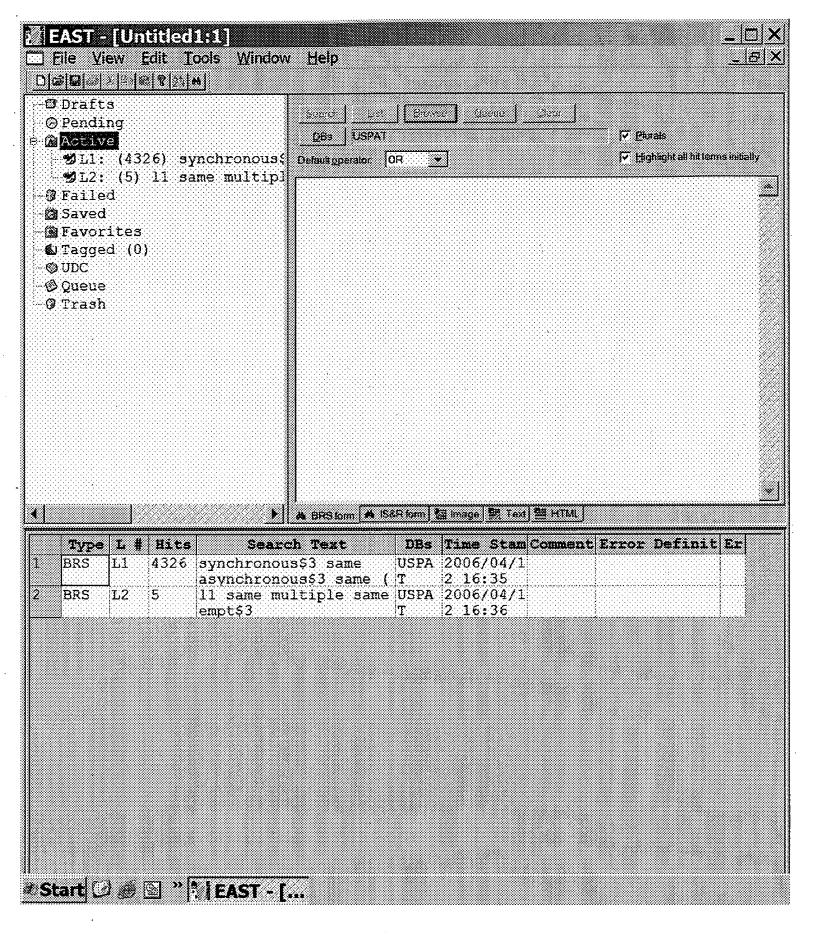
L4 L1 same multiple

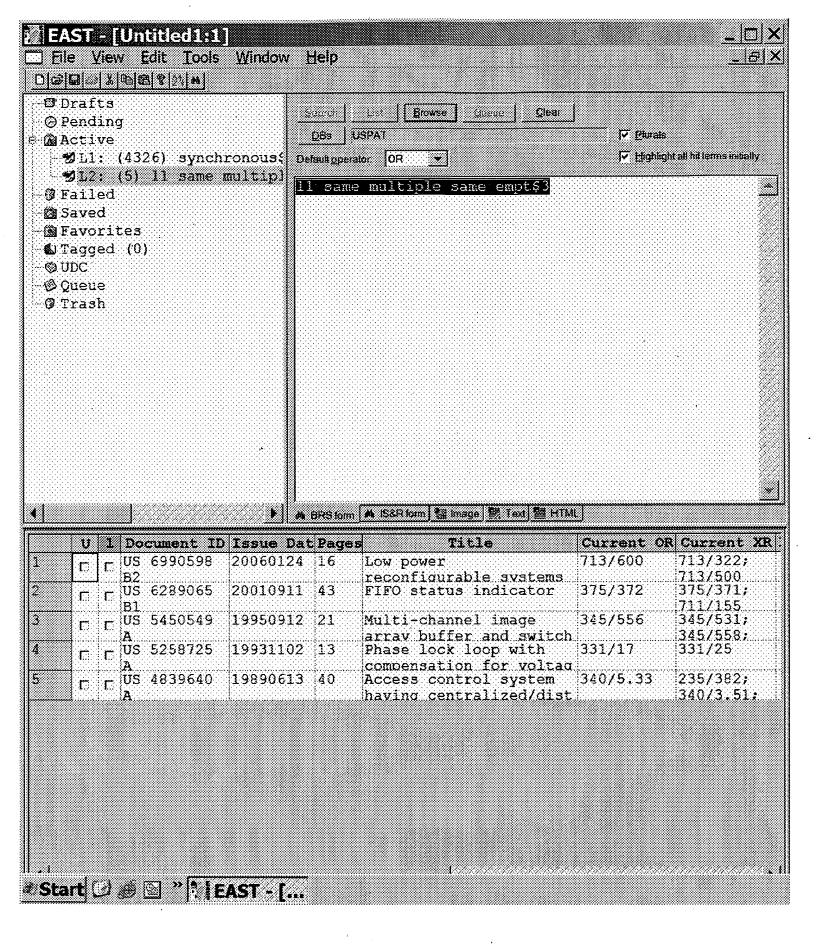
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	Lloyd, D.W.; Gar Advanced Resea 19-21 April 1999	n asynchronous microprocessors side, J.D.; Gilbert, D.A.; urch in Asynchronous Circuits and S Page(s):71 - 80 entifier 10.1109/ASYNC.1999.76152	ystems 1999 Proceedings, Fifth	h International Symposium on
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## Memory faults in asynchronous microprocessors

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This paper appears in: Advanced Research in Asynchronous Circuits and Systems, 1999. Proceedings, Fifth International

#### Symposium on

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#### Abstract

Although a large number of asynchronous microprocessors have now been designed, relatively few have attempted to handle memory faults. Memory faults create problems for the design of any pipelined system which are exacerbated by the non-deterministic nature of an asynchronous processor. This paper describes these problems as encountered in the design of asynchronous ARM processors and discusses their specific solutions in the AMULET3 processor. Different mechanisms were used, as expedient, to maintain coherency for the various state-holding elements within the processor; these include register renaming and history buffering in addition to resource locking

#### Index Terms

Inspec

#### Controlled Indexing

asynchronous circuits buffer storage microprocessor chips pipeline processing

## Non-controlled Indexing

AMULET3 processor ARM processors asynchronous microprocessors history buffering memory faults pipelined system register renaming resource locking

### **Author Keywords**

Not Available

References

No references available on IEEE Xplore.

Citing Documents

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